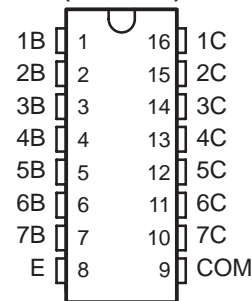


HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 100 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay Driver Applications
- Higher-Voltage Versions of ULN2003A and ULN2004A, for Commercial Temperature Range

SN75468 . . . D, N, OR NS PACKAGE
SN75469 . . . D OR N PACKAGE

(TOP VIEW)



description/ordering information

The SN75468 and SN75469 are high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The SN75468 has a 2700- Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS. The SN75469 has a 10.5-k Ω series base resistor to allow its operation directly with CMOS or PMOS that use supply voltages of 6 to 15 V. The required input current is below that of the SN75468.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	SN75468N	SN75468N
	SOIC (D)	Tube of 40	SN75468D	SN75468
		Reel of 2500	SN75468DR	
	SOP (NS)	Reel of 2000	SN75468NSR	SN75468
	PDIP (N)	Tube of 25	SN75469N	SN75469N
	SOIC (D)	Tube of 40	SN75469D	SN75469
Reel of 2500		SN75469DR		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



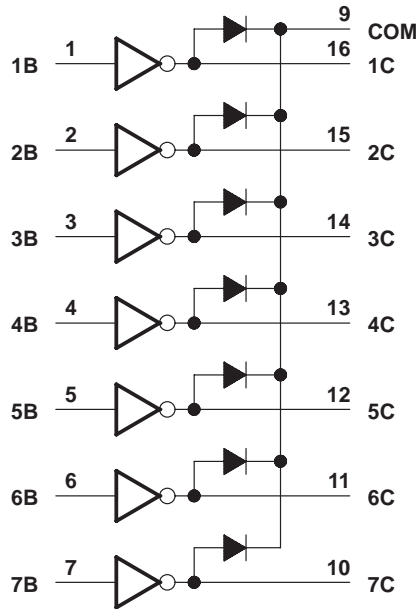
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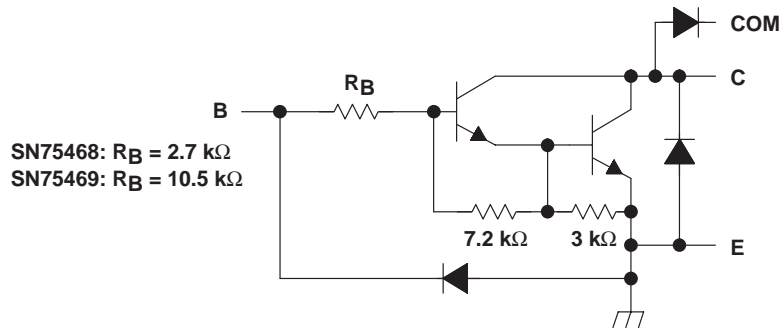
SN75468, SN75469 DARLINGTON TRANSISTOR ARRAYS

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logic diagram



schematic (each Darlington pair)



All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Collector-emitter voltage, V_{CE}	100 V
Input voltage, V_I (see Note 1)	30 V
Peak collector current (see Figures 14 and 15)	500 mA
Output clamp current, I_{OK}	500 mA
Total emitter-terminal current	–2.5 A
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package	73°C/W
N package	67°C/W
NS package	64°C/W
Operating virtual junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
 2. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

SN75468, SN75469 DARLINGTON TRANSISTOR ARRAYS

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electrical characteristics, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	SN75468			SN75469			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(\text{on})}$ On-state input voltage	5	$V_{CE} = 2\text{ V}$	$I_C = 125\text{ mA}$					5	V
			$I_C = 200\text{ mA}$			2.4		6	
			$I_C = 250\text{ mA}$			2.7			
			$I_C = 275\text{ mA}$					7	
			$I_C = 300\text{ mA}$			3			
			$I_C = 350\text{ mA}$					8	
$V_{CE(\text{sat})}$ Collector-emitter saturation voltage	6	$I_I = 250\ \mu\text{A}$, $I_C = 100\text{ mA}$	0.9	1.1	0.9	1.1		V	
		$I_I = 350\ \mu\text{A}$, $I_C = 200\text{ mA}$	1	1.3	1	1.3			
		$I_I = 500\ \mu\text{A}$, $I_C = 350\text{ mA}$	1.2	1.6	1.2	1.6			
V_F Clamp-diode forward voltage	8	$I_F = 350\text{ mA}$	1.7	2	1.7	2		V	
I_{CEX} Collector cutoff current	1	$V_{CE} = 100\text{ V}$, $I_I = 0$		50		50		μA	
		$V_{CE} = 100\text{ V}$, $I_I = 0$		100		100			
	2	$T_A = 70^\circ\text{C}$, $V_I = 1\text{ V}$				500			
$I_{I(\text{off})}$ Off-state input current	3	$V_{CE} = 50\text{ V}$, $T_A = 70^\circ\text{C}$, $I_C = 500\ \mu\text{A}$	50	65	50	65		μA	
I_I Input current	4	$V_I = 3.85\text{ V}$	0.93	1.35				mA	
		$V_I = 5\text{ V}$			0.35	0.5			
		$V_I = 12\text{ V}$			1	1.45			
I_R Clamp-diode reverse current	7	$V_R = 100\text{ V}$		50		50		μA	
		$V_R = 100\text{ V}$, $T_A = 70^\circ\text{C}$		100		100			
C_i Input capacitance		$V_I = 0$, $f = 1\text{ MHz}$	15	25	15	25		pF	

switching characteristics, $T_A = 25^\circ\text{C}$ free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$V_S = 50\text{ V}$, $R_L = 163\ \Omega$, $C_L = 15\text{ pF}$,		0.25	1	μs
t_{PHL} Propagation delay time, high-to-low-level output	See Figure 9		0.25	1	μs
V_{OH} High-level output voltage after switching	$V_S = 50\text{ V}$, $I_O \approx 300\text{ mA}$, See Figure 10	$V_S - 20$			mV



PARAMETER MEASUREMENT INFORMATION

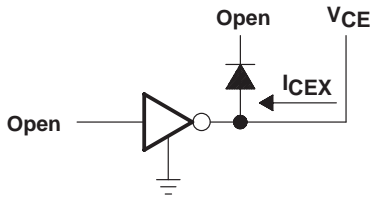


Figure 1. $I_{C EX}$

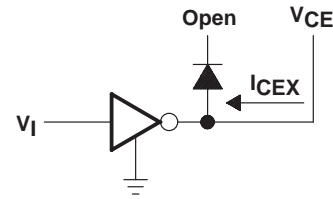


Figure 2. $I_{C EX}$

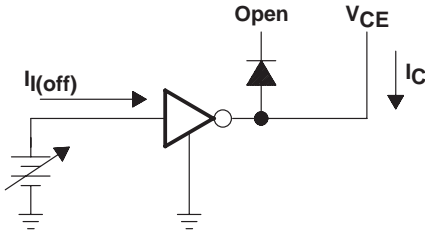


Figure 3. $I_{I(off)}$

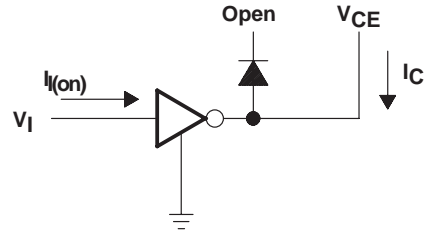


Figure 4. I_I

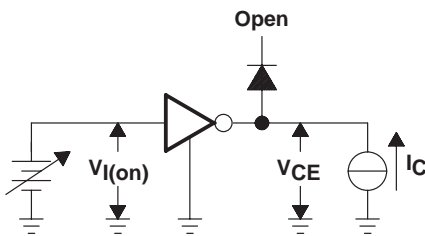
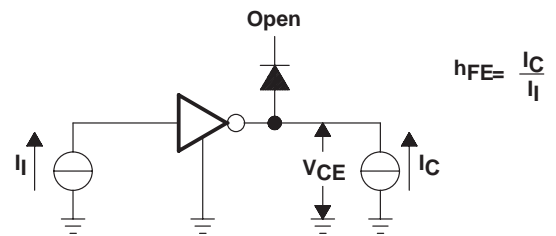


Figure 5. $V_{I(on)}$



NOTE: I_I is fixed for measuring $V_{CE(sat)}$,
 variable for measuring h_{FE} .

Figure 6. h_{FE} , $V_{CE(sat)}$

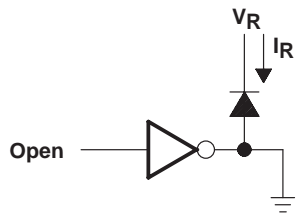


Figure 7. I_R

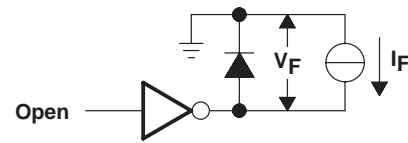


Figure 8. V_F

SN75468, SN75469 DARLINGTON TRANSISTOR ARRAYS

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PARAMETER MEASUREMENT INFORMATION

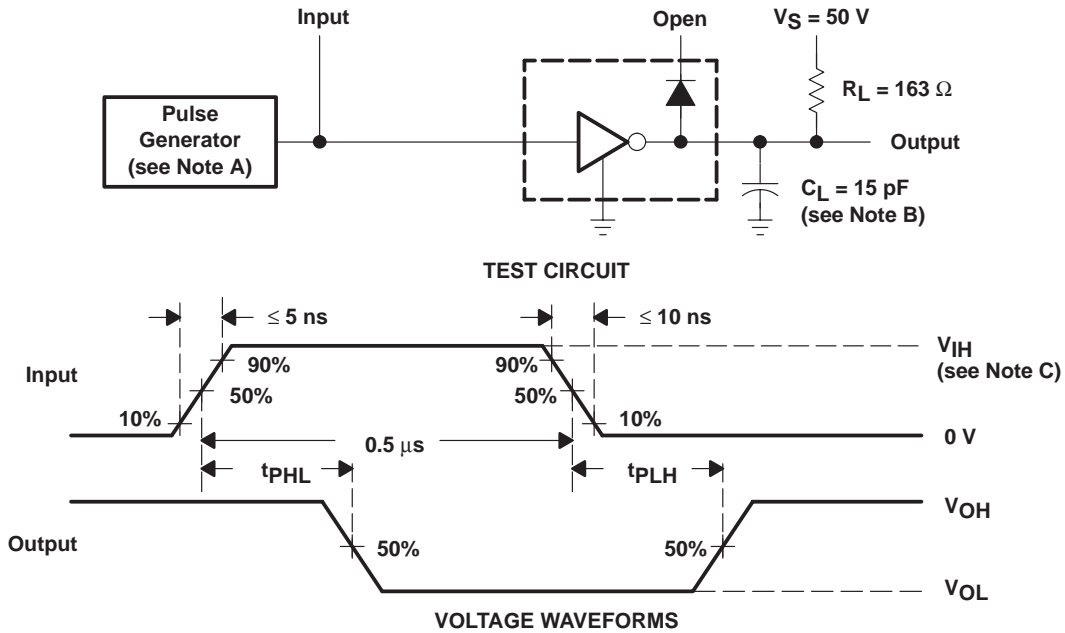


Figure 9. Test Circuit and Voltage Waveforms

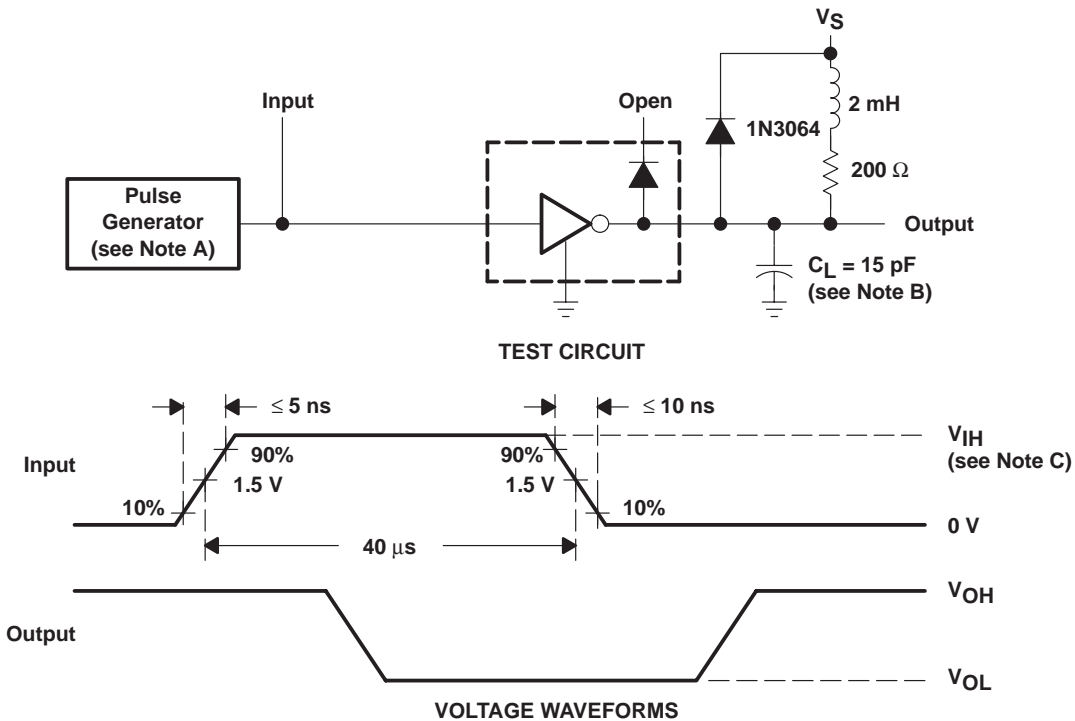


Figure 10. Latch-Up Test Circuit and Voltage Waveforms

- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.
 C. For testing the '468, $V_{IH} = 3 \text{ V}$; for the '469, $V_{IH} = 8 \text{ V}$.

TYPICAL CHARACTERISTICS

**COLLECTOR-EMITTER SATURATION VOLTAGE
 vs
 COLLECTOR CURRENT
 (ONE DARLINGTON)**

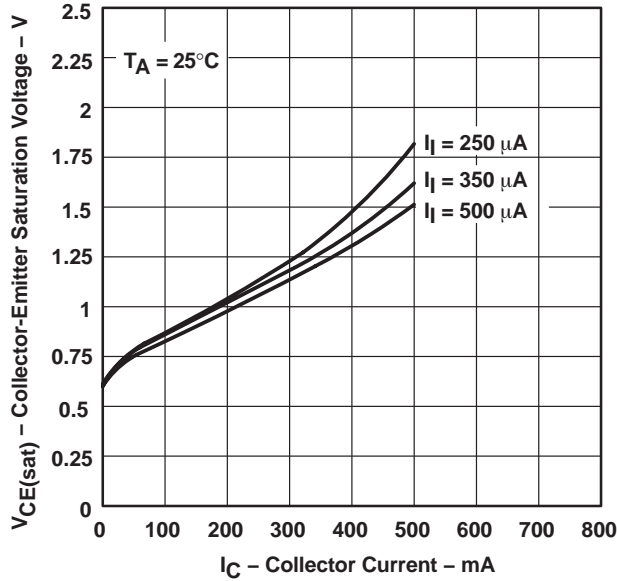


Figure 11

**COLLECTOR-EMITTER SATURATION VOLTAGE
 vs
 COLLECTOR CURRENT
 (TWO DARLINGTONS PARALLELED)**

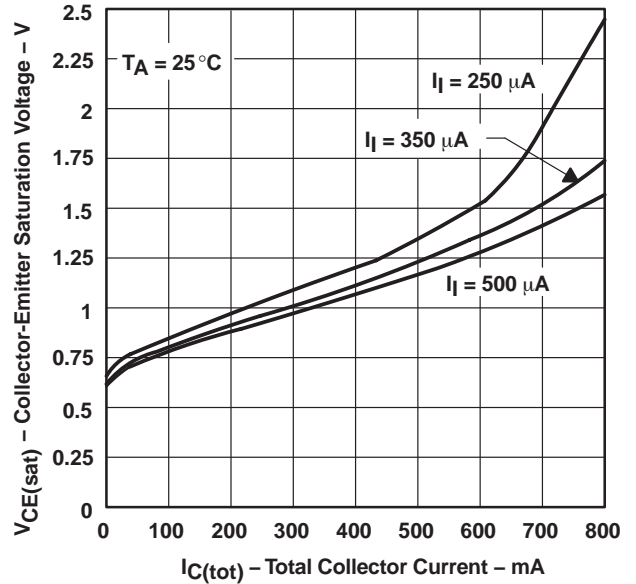


Figure 12

**COLLECTOR CURRENT
 vs
 INPUT CURRENT**

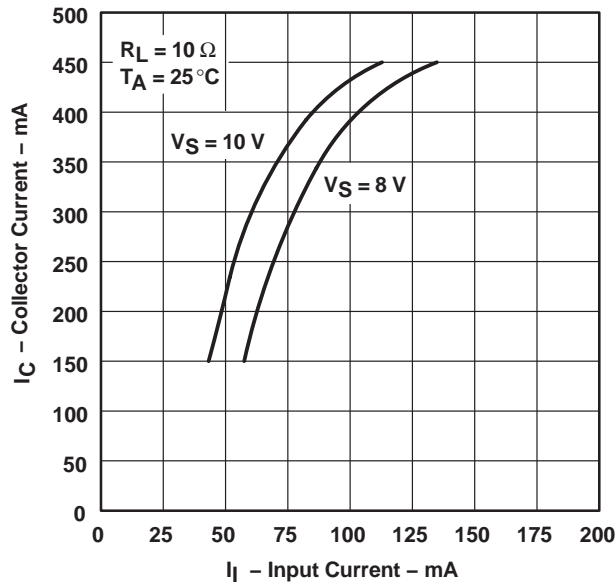


Figure 13

**SN75468, SN75469
DARLINGTON TRANSISTOR ARRAYS**

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THERMAL INFORMATION

**D PACKAGE
MAXIMUM COLLECTOR CURRENT
VS
DUTY CYCLE**

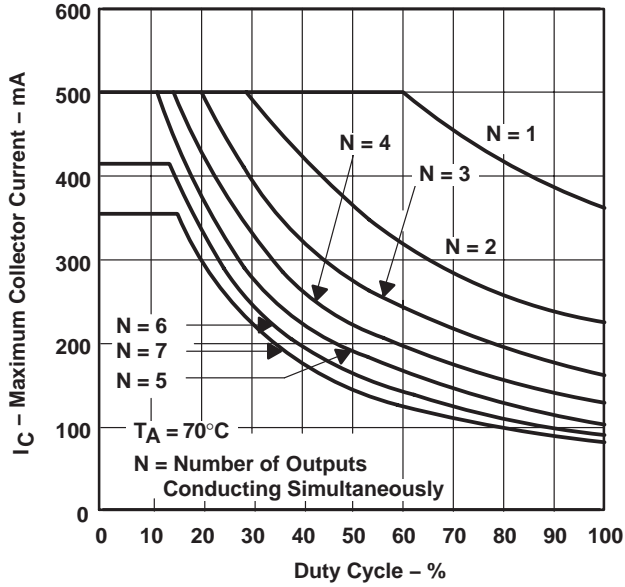


Figure 14

**N PACKAGE
MAXIMUM COLLECTOR CURRENT
VS
DUTY CYCLE**

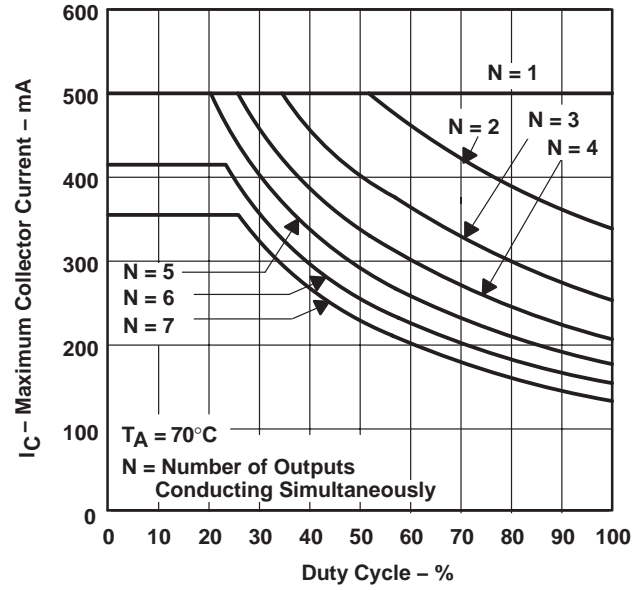


Figure 15

APPLICATION INFORMATION

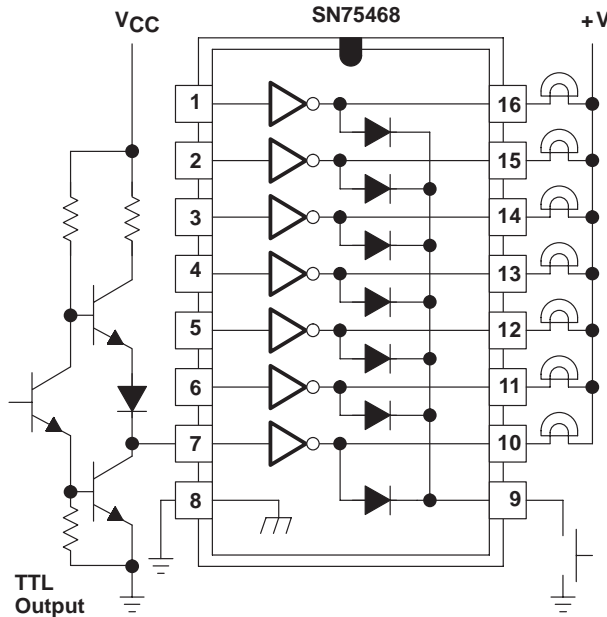


Figure 16. TTL to Load

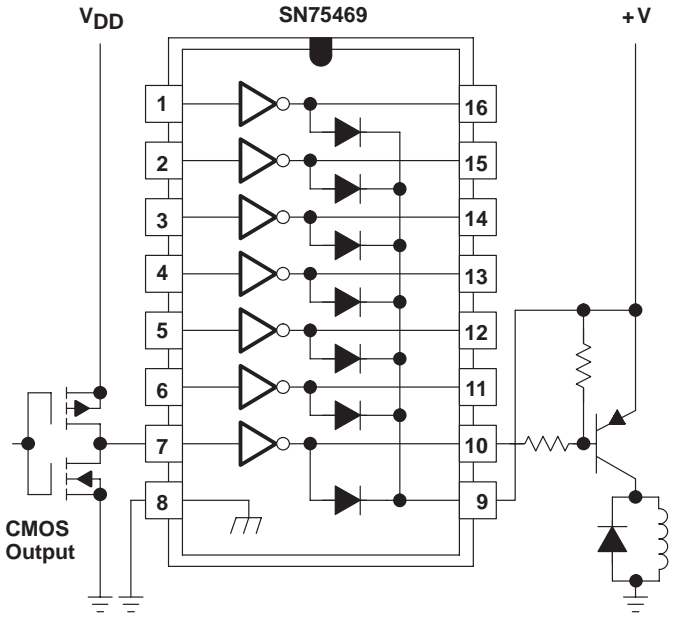


Figure 17. Buffer for Higher Current Loads

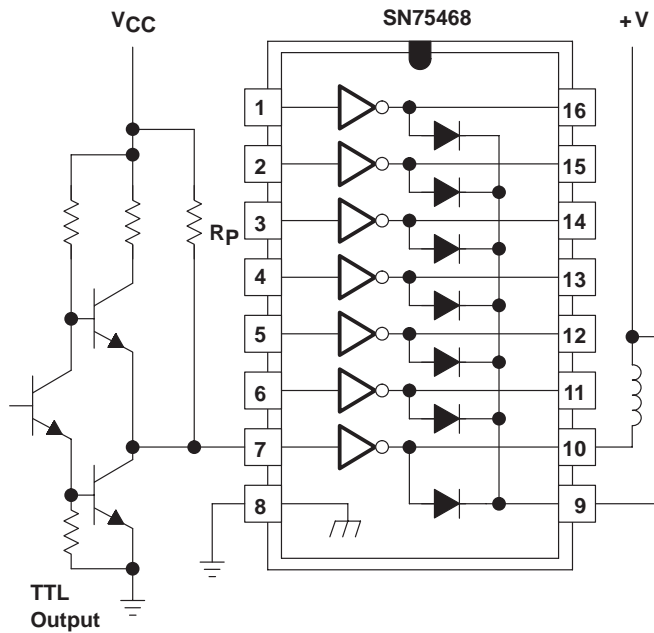


Figure 18. Use of Pullup Resistors to Increase Drive Current

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75468D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75468DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75468DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75468DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75468DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75468DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75468N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75468NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75468NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75468NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75468NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75469D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75469DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75469DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75469DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75469DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75469DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75469N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75469NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75468NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75469DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75468NSR	SO	NS	16	2000	346.0	346.0	33.0
SN75469DR	SOIC	D	16	2500	333.2	345.9	28.6

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

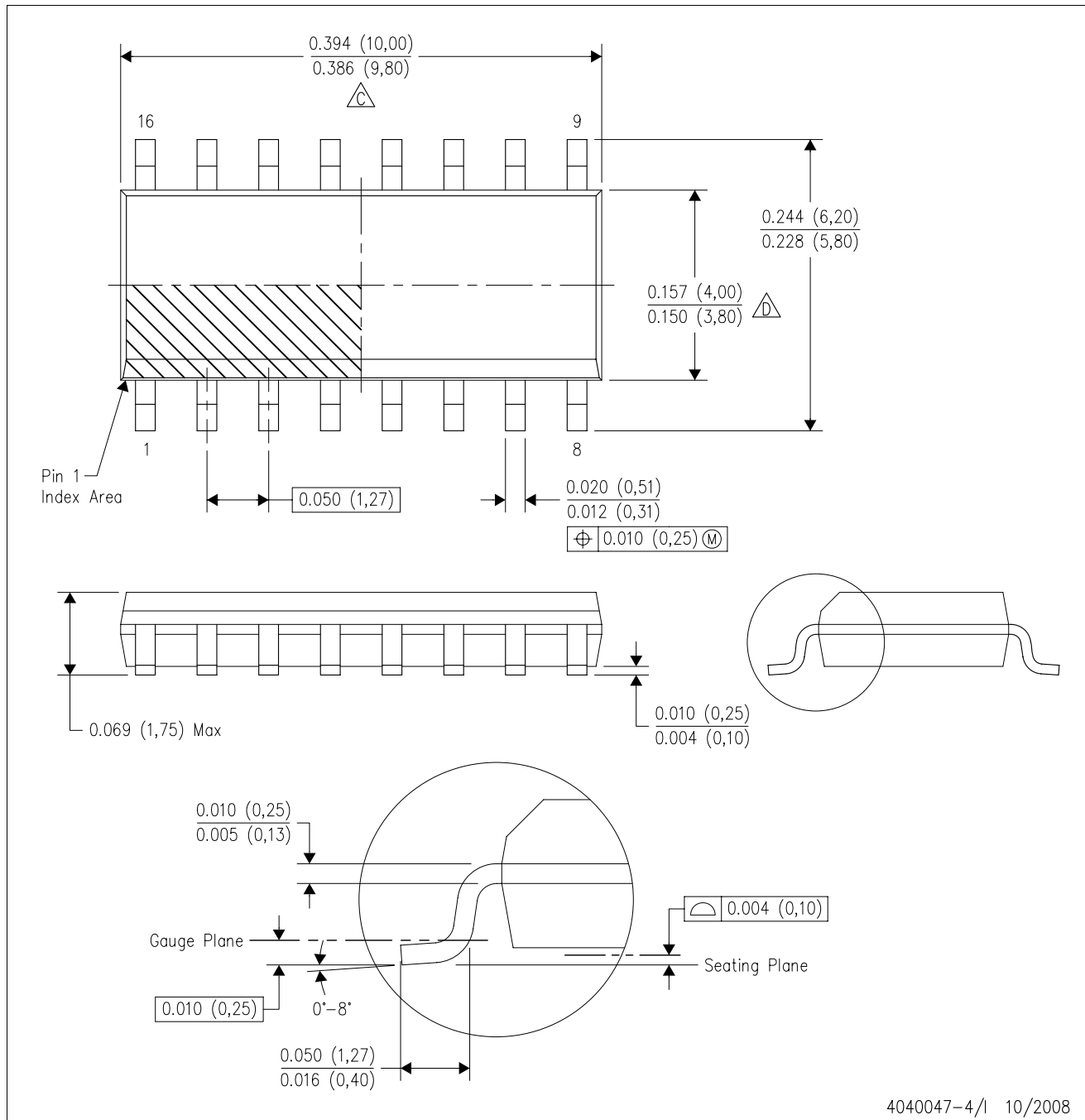
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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Security	www.ti.com/security
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